AMENDMENTS TO THE CLAIMS

Claim 1 (Currently Amended) A phase locked loop circuit, comprising

a phase comparator for comparing phases of an index signal and a reference signal and outputting a signal in accordance with the phase difference;

a loop filter for smoothing the output signal of the phase comparator;

a controlled oscillator for oscillating at a frequency in accordance with an ~~the~~ output signal of the loop filter;

a limiter provided on a path from the output side of the phase comparator to the input side of the controlled oscillator for limiting the level of signals on the path in a predetermined range of phase differences and setting a large gain;

a frequency divider for dividing an ~~the~~ output signal of the controlled oscillator by a predetermined frequency dividing rate N (where N is a positive integer), generating the reference signal and feedback-inputting the reference signal to the phase comparator;

an unlock detecting circuit for ~~outputting the~~ detecting unlocking of a phase lock based on the index signal and the reference signal or based on the output signal of the phase comparator and for outputting an unlock detecting signal; and

a switch unit for shutting up the output signal of the loop filter based on ~~the unlock detecting~~ a PLL operational signal and inputting a predetermined signal to the controlled oscillator.

Claim 2 (Currently Amended) A phase locked loop circuit, comprising

a phase comparator for comparing phases of an index signal and a reference signal and outputting a signal in accordance with the phase difference;

a lead-in start signal generating circuit for generating a lead-in start signal in response to the index signal ~~input~~ at the start of an operation;

a loop filter for smoothing the output signal of the phase comparator;

a controlled oscillator for oscillating at a frequency in accordance with ~~the~~ an output signal of the loop filter;

a frequency divider for generating the reference signal having the minimum phase difference with respect to the index signal when the lead-in start signal is input, feedback-inputting the reference signal to the phase comparator, generating the reference signal by dividing the output signal of the controlled oscillator by a predetermined frequency dividing rate N (where N is a positive integer) when ~~the~~ an output signal of the controlled oscillator is input, and feedback-inputting the reference signal to the phase comparator;

an unlock detecting circuit for detecting the unlocking of a phase lock based on the index signal and the reference signal or based on the output signal of the phase comparator and for outputting an unlock detecting signal; and

a switch unit for shutting up the output signal of the loop filter based on ~~the unlock detecting~~ a PLL operational signal and inputting a predetermined signal to the controlled oscillator.

Claim 3 (Currently Amended) A phase locked loop circuit, comprising

a phase comparator for comparing phases of an index signal and a reference signal and outputting a signal in accordance with the phase difference;

a lead-in start signal generating circuit for generating a lead-in start signal in response to the index signal ~~input~~ at the start of an operation;

a loop filter for smoothing the output signal of the phase comparator;

a controlled oscillator for oscillating at a frequency in accordance with ~~the~~ an output signal of the loop filter;

a limiter provided on a path from the output side of the phase comparator to the input side of the controlled oscillator for limiting the level of signals on the path in a predetermined range of phase differences and setting a large gain;

a frequency divider for generating the reference signal having the minimum phase difference with respect to the index signal when the lead-in start signal is input, feedback-inputting the reference signal to the phase comparator, generating the reference signal by dividing the output signal of the controlled oscillator by a predetermined frequency dividing rate N (where N is a positive integer)

when ~~the~~ an output signal of the controlled oscillator is input, and feedback-inputting the reference signal to the phase comparator;

an unlock detecting circuit for detecting the unlocking of a phase lock based on the index signal and the reference signal or based on the output signal of the phase comparator and for outputting an unlock detecting signal; and

a switch unit for shutting up the output signal of the loop filter based on ~~the unlock detecting~~ a PLL operational signal and inputting a predetermined signal to the controlled oscillator.

Claim 4 (Original) A phase locked loop circuit according to Claim 1, wherein the controlled oscillator is a voltage controlled oscillator or a current controlled oscillator.

Claim 5 (Original) A phase locked loop circuit according to Claim 2, wherein the frequency divider is a preset frequency divider be preset when the lead-in start signal is input.